UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,494	02/06/2002	Taeg-Hyun Kang	40013.001	1924

27966 7590 05/18/2007

KENNETH E. HORTON
KIRTON & MCCONKLE
60 EAST SOUTH TEMPLE
SUITE 1800
SALTLAKE CITY, UT 84111

EXAMINER	
MANDALA, VICTOR A	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
05/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/071,494
Filing Date: February 06, 2002
Appellant(s): KANG ET AL.

Fairchild Semiconductor, Ltd. by virtue of two Assignments from the inventors to Fairchild Semiconductor Corporation and then from that entity to Fairchild Korea Semiconductor, Ltd.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1/16/07 appealing from the Office action mailed 3/28/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,623,154	Murakami et al.	04-1997
6,841,821	Hsu	01-2005
3,789,503	Nishida et al.	02-1974

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-10, 19-29, 40, and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

1. Independent claims 1, 19, 27, 29, 40, and 41 have a limitation of no thin gate oxide, which is found to be indefinite because of the meaning of thin. What would the reference point be to define what thin would be? How thick would an oxide be to be not thin?

Claims 1-4, 7-10, 19, 23, 26, 27, and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,623,154 Murakami et al.

2. Referring to claim 1, a field transistor having a current a path between a source and a drain while containing no gate insulating layer, (See 112 rejection above), the transistor comprising: a well region of a first conductivity type, (Figure 1 #20); a field oxide layer, (Figure 1 #15 and Col. 8 Lines 27-29 where the gate oxide layer is made by thermal oxidation, which is the same method of making as an isolation FOX layer), for defining an active region, (Figure 1 area of #20), on the well region, (Figure 1 #20); high concentration source and drain regions of a second conductivity type, (Figure 1 #9), separated from each other by a width of the field oxide layer, (Figure 1 #15); a low concentration source region of the second conductivity type, (Figure 1 #7), formed in the well region, (Figure 1 #20), the low concentration source, (Figure 1 #7), region being adjacent to the high concentration source region, (Figure 1 #9), and overlapped by one end of the field oxide layer, (Figure 1 #15); a low concentration drain region of the second

conductivity type, (Figure 1 #7), formed in the well region, (Figure 1 #20), the low concentration drain region, (Figure 1 #7), being adjacent to the high concentration drain region, (Figure 1 #9), and overlapped by the other end of the field oxide layer, (Figure 1 #15); and a gate conductive layer pattern formed on the field oxide layer, (Figure 1 #15), the gate conductive layer pattern, (Figure 1 #17), overlapping parts of the low concentration source and drain regions of the second conductivity type, (Figure 1 #7).

3. Referring to claim 2, a field transistor, wherein the well region, (Figure 1 #20), of the first conductivity type is formed on a high concentration buried region, (Figure 1 #3), of the first conductivity type on a semiconductor substrate, (Figure 1 #1), of the first conductivity type.

4. Referring to claim 3, a field transistor, wherein the well region, (Figure 1 #20), of the first conductivity type is formed on a semiconductor substrate, (Figure 1 #1), of the first conductivity type.

5. Referring to claim 4, a field transistor, further comprising a high concentration diffusion region, (Figure 1 #3), of the first conductivity type formed in the well region, (Figure 1 #20), the high concentration diffusion region, (Figure 1 #3), being separated from the high concentration source region, (Figure 1 #9), of the second conductive type by a predetermined distance.

6. Referring to claim 7, a field transistor, further comprising: a gate electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the gate conductive layer pattern, (Figure 1 #17); a source electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the high concentration source region, (Figure 1 #9), of the second conductivity type; and a drain electrode, (It is apparent there

would be an electrode in order for the device to work), electrically connected to the high concentration drain region, (Figure 1 #9), of the second conductivity type.

7. Referring to claim 10, a field transistor, wherein the first conductivity type is p-type, and the second conductivity type is n-type, (Figure 1).

8. Referring to claim 19, a semiconductor device having a current path between a source and a drain while containing no thin gate insulating layer, (See 112 rejection above), the transistor comprising: a substrate, (Murakami et al. Figure 1 #1), comprising a well region of a first conductivity type, (Murakami et al. Figure 1 #20); a field oxide layer, (Murakami et al. Figure 1 #15 and Col. 8 Lines 27-29 where the gate oxide layer is made by thermal oxidation, which is the same method of making as an isolation FOX layer), located over a portion of the well region, (Murakami et al. Figure 1 #20); a first source region of a second conductivity type, (Murakami et al. Figure 1 #9), and a first drain region of a second conductivity type, (Murakami et al. Figure 1 #9), separated by the field oxide layer, (Murakami et al. Figure 1 #15); a second source region having a second conductivity type concentration lower, (Murakami et al. Figure 1 #7), than the first source region, (Murakami et al. Figure 1 #9), the second source region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first source region, (Murakami et al. Figure 1 #9), with a portion of the second source region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); a second drain region having a second conductivity type concentration lower, (Murakami et al. Figure 1 #7), than the first drain region, (Murakami et al. Figure 1 #9), the second drain region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first drain region, (Murakami et al. Figure 1 #9), with a portion of the

second drain region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); and a conductive layer, (Murakami et al. Figure 1 #17), formed over the field oxide layer, (Murakami et al. Figure 1 #15), the conductive layer, (Murakami et al. Figure 1 #17), overlapping the second source region, (Murakami et al. Figure 1 #7), and the second drain region, (Murakami et al. Figure 1 #7).

9. Referring to claim 23, a device, further comprising: a gate electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the conductive layer, (Figure 1 #17); a source electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the first source region, (Figure 1 #9); and a drain electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the first drain region, (Figure 1 #9).

10. Referring to claim 26, a device, wherein the first conductivity type is p-type and the second conductivity type is n-type, (Figure 1).

11. Referring to claim 27, a semiconductor device having a current path between a source and a drain while containing no thin gate insulating layer, (See 112 rejection above), the transistor comprising: a substrate, (Murakami et al. Figure 1 #1), comprising a well region of a first conductivity type, (Murakami et al. Figure 1 #20); a field oxide layer, (Murakami et al. Figure 1 #15 and Col. 8 Lines 27-29 where the gate oxide layer is made by thermal oxidation, which is the same method of making as an isolation FOX layer), located over the well region, (Murakami et al. Figure 1 #20); a first source region of a second conductivity type, (Murakami et al. Figure 1 #9), and a first drain region of a second conductivity type, (Murakami et al. Figure 1 #9), separated by the field oxide layer, (Murakami et al. Figure 1 #15); a second source region

having a second conductivity type, (Murakami et al. Figure 1 #7), concentration lower than the first source region, (Murakami et al. Figure 1 #9), the second source region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first source region, (Murakami et al. Figure 1 #9), with a portion of the second source region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); a second drain region having a second conductivity type, (Murakami et al. Figure 1 #7), concentration lower than the first drain region, (Murakami et al. Figure 1 #9), the second drain region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first drain region, (Murakami et al. Figure 1 #9), with a portion of the second drain region underlying the field oxide layer, (Murakami et al. Figure 1 #15); a conductive layer formed over the field oxide layer, (Murakami et al. Figure 1 #15), the conductive layer, (Murakami et al. Figure 1 #17), overlapping the second source region, (Murakami et al. Figure 1 #7), and the second drain region, (Murakami et al. Figure 1 #7); a gate electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the conductive layer, (Murakami et al. Figure 1 #17); a source electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the first source region, (Murakami et al. Figure 1 #9); and a drain electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the first drain region, (Murakami et al. Figure 1 #9).

12. Referring to claim 29, a system for electrostatic discharge protection containing a field transistor having a current path between a source and a drain without a thin gate insulating layer, (See 112 rejection above), the field transistor comprising: a substrate, (Murakami et al. Figure 1 #1), comprising a well region of a first conductivity type, (Murakami et al. Figure 1 #20); a field

oxide layer, (Murakami et al. Figure 1 #15 and Col. 8 Lines 27-29 where the gate oxide layer is made by thermal oxidation, which is the same method of making as an isolation FOX layer), located over the well region, (Murakami et al. Figure 1 #20); a first source region of a second conductivity type, (Murakami et al. Figure 1 #9), and a first drain region of a second conductivity type, (Murakami et al. Figure 1 #9), separated by the field oxide layer, (Murakami et al. Figure 1 #15); a second source region having a second conductivity type, (Murakami et al. Figure 1 #7), concentration lower than the first source region, (Murakami et al. Figure 1 #9), the second source region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first source region, (Murakami et al. Figure 1 #9), with a portion of the second source region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); a second drain region having a second conductivity type, (Murakami et al. Figure 1 #7), concentration lower than the first drain region, (Murakami et al. Figure 1 #9), the second drain region formed, (Murakami et al. Figure 1 #7), in the well region, (Murakami et al. Figure 1 #20), adjacent the first drain region, (Murakami et al. Figure 1 #9), with a portion of the second drain region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); and a conductive layer, (Murakami et al. Figure 1 #17), formed over the field oxide layer, (Murakami et al. Figure 1 #15), the conductive layer, (Murakami et al. Figure 1 #17), overlapping the second source region, (Murakami et al. Figure 1 #7), and the second drain region, (Murakami et al. Figure 1 #7).

(10) Response to Argument

A. The Applicant argues that the 35 USC 112 2nd paragraph rejection of claims 1-10, 19-29, 40, and 41 does not meet the three criteria's as stated in MPEP §2173.02. MPEP §2173.02 states the definiteness of a claim language must be analyzed, not in a vacuum, but in light of: (i) the content of the particular application disclosure; (ii) the teachings of the prior art; and (iii) the claim interpretation that would be given by one possessing the ordinary skill in the art at the time the invention was made. The Applicant further argues the rejection in regard to i, ii, and iii.

i. The Applicant argues that the specification does not provide an exact thickness or range of thickness for the thin gate insulator, but would be reasonable to one skilled in the art, (Appeal Brief page 15 lines 4-6). The Applicant continues and states the specification describes the function of the device would enable one having skill to determine the range of thicknesses for the thin gate oxide, (Appeal Brief page 15 lines 1-4). The examiner has considered these arguments but finds them to be non-persuasive. The term "no thin gate oxide" is found to be indefinite in this case because the disclosure does not teach any numeric limitations on what the thickness of the oxide is, which would be used as a reference point defining between thin and thick. Nowhere is it taught and nowhere can it be assumed what the limitation of "no thin gate oxide" is meant by. The examiner also does not have the means to determine the range of thicknesses that would determine the definition of thin gate oxide by experimentation. The current view of the courts is that there is nothing inherently ambiguous or uncertain about a negative limitation. So long as the boundaries of the patent protection sought are so forth definitely, albeit negatively, the claim complies with the 35 USC 112, second paragraph. Some older cases were critical of negative limitations because they tended to define the invention in

terms of what it was not, rather than pointing out the invention. Thus, the court observed that the limitation "R is an alkenyl radical other than 2-butenyl and 2, 4-pentadienly" was a negative limitation that rendered the claim indefinite because it was an attempt to claim the invention by excluding what the inventors did not invent rather than distinctly and particularly pointing out what they did invent. In re Schechter, 205 F.2d 185, 98 USPQ 144 (CCPA 1953). A claim which recited the limitation "said homopolymer being free from the proteins, soaps, resins, and sugars present in natural Hevea rubber" in order to exclude the characteristics of the prior art product, was considered definite because each recited limitation was definite. In re Wakefield, 422 F.2d 897, 899, 904, 164 USPQ 636, 638, 641 (CCPA 1970). This instant case the limitation of no thin gate oxide relates to In re Schechter because the claim is attempting to claim the invention by excluding what the inventor did not invent rather than distinctly and particularly pointing out what they did invent.

ii. The Applicant's argues on the basis of the limitation "no thin gate oxide" as being definite because of a word search from a patent search engine, which generated 42 results. The Applicant continues to argue that the Patent Office did not find those terms to be indefinite for the 42 cases found by the Applicant. The examiner has considered these arguments, but finds them to be non-persuasive. The mere citing of 42 results of a search engine do not truly depict what each of the disclosures teach and/ or what is taught in the estoppel of each of the results. The rejection is made on a case-by-case basis. The Applicant continues to argue that the cited references, (U.S. Patent No. 3,789,503 Nishida et al. and U.S. Patent No. 6,841,821 Hu et al.), filed in the final office action on 3/28/05 is not legally or factually sufficient to support the argument of existence of a wide disparity of thickness for a thin gate oxide layer. The Applicant

also states, " The time frame for inquiring about indefiniteness is as noted above at the time of the invention", Appeal Brief page 15 lines 18-20. The examiner has considered the arguments but finds them to be non-persuasive because the cited references where used to show examples which provided a difference of almost 1,600 Angstroms between one definition of thin gate oxide to another. It would be improper for the examiner to assume a definite meaning for the term thin gate oxide, where there are multiple definitions for the term as taught by Nishida et al. and Hsu. The Nishida et al. patent was published in 1974 but was only used as an example to show how the definition of a thin gate oxide is always evolving and is changing at an accelerated rate. The Applicant also states this fact on page 16 lines 1-2, where, "as any skilled artisan can testify, the size and dimensions of semiconductor devices have been decreasing for many years and this knowledge is recognized even outside the semiconductor art." This disparity proves that a definite definition of a thin gate oxide from the prior art can not be determined, since the definition has been changing so rapidly.

The Applicant has provided evidence that U.S. Patent No. 6,586,306 has claimed limitations stating where a thin gate oxide is in one region and a thick gate oxide is in another region. The Applicant continues to argue that the specification does not disclose a numerical range for the terms thin and thick, yet the application was allowed. The examiner has considered the Applicant's arguments but finds them to be non-persuasive because as stated previously the definition and definiteness is based on a case-by-case basis. This case has in fact defined a definite definition for the terms thin and thick because a reference point has been established which can be defined by the thin gate oxide has less of a thickness than the thick gate oxide and where both elements, thin and thick gate oxides, are in the claim and in the device. The current

claim does not recite two elements where the definition of thin gate oxide can be determined by comparison of an other element such as a thick gate oxide, hence lacking a reference point which would enable a skilled artesian to determine the definition of thin.

iii. The Applicant states that the declaration under 37 CFR 1.132 was not entered and considered by the examiner on 8/9/05. The applicant also states that the Advisory Action indicates that the affidavit was file after the date of filing a Notice of Appeal. The examiner has considered these statements and has found the After final has stated the filing of the affidavit was file after the date of filing a Notice of Appeal was an error and where the After final should have stated that the affidavit was file after a final action, but before or on the date of filing a Notice of Appeal. The other statements in the Advisory Action are correct in regard to the affidavit will not be entered because Applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e). The Affidavit filed on 6/30/05 does not provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented, hence the affidavit was not entered. The Applicant also states on page 5 lines 18-20 and page 6 lines 1-2, where it only states that the definiteness inquiry does not depend only one what different numerical ranges can be found in the prior art, but, "must also be considered whether a skilled artisan would have understood whether the skilled artisan would have understood whether this claim term sets out and circumscribes a particular subject matter with a reasonable degree of clarity and particularity." The affidavit does not provide any reason what the particular subject matter is that the skilled artisan would provide and its clarity to the arguments at hand, hence viewed as open ended and insufficient. The Applicant also argues that the examiner has not met the

requisite burden of showing that the thin gate oxide layer would render the claims indefinite to the skill artisan. The examiner has considered this argument and finds it to be non-persuasive because of the previously stated evidence, which can be found in i and ii. It is the responsibility of the Applicant to provide a definite limitation, where the examiner is able to search and provide if any a novel conclusion as stated by 35 U.S.C. 112 second paragraph. The 35 U.S.C. 112 second paragraph rejection on claims 1-10 19-29, 40, & 41 stands as is.

B. The Applicant argues that the 35 USC 102 (b) rejection of claims 1-4, 7-10, 19, 23, 26, 27, and 29 as anticipated by U.S. Patent No. 5,623,154 to Murakami does not teach all of the claimed limitations, such as no thin gate oxide. The Applicant also continues to argue that the reference is not capable of protecting a device form ESD because the gate oxide is a thin gate oxide. The Applicant also points out that the reference labels the oxide layer in the device to be a thin gate oxide. The examiner has considered the Applicant's arguments, but finds them to be non-persuasive because as stated in the 35 USC 112 2nd paragraph rejection and in the arguments that the limitation thin gate oxide is indefinite and the examiner is unable to determine a structural difference from the device taught by Murakami. Murakami teaches a structure that contains all of the physical structures that the independent claims claim. The claim does not recite a definite definition of thin gate oxide, which would decipher it from the gate oxide at hand in Murakami's device and where Murakami's device is capable of protecting a device from ESD by an unspecified amount which is dependent on the thickness of the gate oxide, yet there is nothing in the claim or in the specification that would structurally define a device different from Murakami's. The 35 USC 102 (b) rejection of claims 1-4, 7-10, 19, 23, 26, 27, and 29 as anticipated by U.S. Patent No. 5,623,154 to Murakami stands as is.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

An appeal conference was held on 11/28/06 with Mr. Victor A. Mandala Jr (Patent Examiner), Ricky Mack, (Supervisory Patent Examiner), and Leonardo Andujar, (Acting Supervisory Examiner), as the conferees.

Respectfully submitted,

Ricky Mack (Conferee)
Acting Supervisory Examiner
Art Unit 2873

Victor A. Mandala Jr
Patent Examiner
Art Unit 2826

Leonardo Andujar (Conferee)
Acting Supervisory Examiner
Art Unit 2826